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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,068	04/20/2006	Yasuhiro Suzuki	46124-5391	4269

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EXAMINER	
BEMBEN, RICHARD M	

ART UNIT	PAPER NUMBER
2622	

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11/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/539,068	SUZUKI ET AL.	
	Examiner	Art Unit	
	RICHARD M. BEMBEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,002,435 issued to Yamamoto et al., hereinafter "Yamamoto".

Regarding **claim 1**, Yamamoto discloses a photodetector comprising:

(K.times.M.times.N) photodiodes PD.sub.k,m,n (K being an integer of no less than 2; k being integers of no less than 1 and no more than K; M being an integer of no less than 1; m being integers of no less than 1 and no more than M; N being an integer of no less than 2; and n being integers of no less than 1 and no more than N), each generating an electric charge by an amount corresponding to an intensity of light incident thereon *(refer to c. 13, ll. 51-60 and Figure 1, "100A", "120")*;

(M.times.N) integrating circuits, one of each being provided in correspondence to K photodiodes PD.sub.k,m,n (k=1 to K) among the (K.times.M.times.N) photodiodes PD.sub.k,m,n and each successively inputting and accumulating the electric charges generated at the K photodiodes PD.sub.k,m,n (k=1 to K) and outputting a voltage that is in accordance with the amount of the accumulated electric charges *(refer to c. 14, ll. 14-19, c. 14, ll. 38-59, and Figure 1, "220")*; and

(M.times.N) filter circuits, one of each being provided in correspondence to each of the (M.times.N) integrating circuits and each reducing the thermal noise component contained in the voltage output from the corresponding integrating circuit and outputting the voltage alter reduction of the thermal noise component *(filter could either be: (1) refer to c. 14, ll. 26-29, c. 15, ll. 11-26, and Figure 1, "230" which performs "impedance conversion" – examiner considers "impedance conversion" a filtering process; (2) alternatively refer to c. 14, ll. 29-31 and Figure 1, "250" which filters out the AC component, hence removing the noise associated w/ the DC component)*.

Regarding **claim 2**, refer to the rejection of claim 1 and Yamoto further discloses CDS circuits, each being arranged between said integrating circuit and said filter circuit, inputting the voltage output from the integrating circuit, and outputting a voltage expressing the fluctuation of the input voltage over a fixed time *(refer to c. 14, l. 60 - c. 15, l. 10 and Figure 1, "230" (note "clamp circuit 230" has exact same structure as Applicant's CDS circuit "30"))*.

Regarding **claim 4**, refer to the rejection of claim 1 and Yamoto further discloses that the (K.times.M.times.N) photodiodes PD.sub.k,m,n are arranged in M rows and (K.times.N) columns either two-dimensionally (when M=2) or one dimensionally (when M=1), with each photodiode PD.sub.k,m,n being positioned at the position of the m-th row and (n+(k-1)N)-th column *(refer to c. 18, ll. 31-65 and Figure 4)*.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamoto in view of US Pub. No. 2002/0051067 filed by Henderson et al., hereinafter "Henderson".

Regarding **claim 3**, Yamoto discloses the photodetector as required by the limitations of claim 1. However, Yamoto does not disclose A/D converters, each inputting the voltage output from said filter circuit, performing A/D conversion on this voltage, and outputting a digital value that is in accordance with this voltage.

Henderson discloses a photodetector comprising per-column A/D converters, each inputting the voltage output from said filter circuit, performing A/D conversion on this voltage, and outputting a digital value that is in accordance with this voltage *(refer to [0035] and Figure 4, "206")*. It would have been obvious to a person having ordinary skill in the art at the time of the invention to incorporate per-column A/D converters as disclosed by Henderson in the photodetector *(with per-column readout architecture, refer to Figure 1)* disclosed by Yamoto since per-column A/D converter architectures have the advantages of low power, low voltage operation *(refer to Henderson, [0010])*.

Alternative Claim Rejections under 35 USC § 102

5. Even if the Applicant does not agree with the 35 U.S.C. 102(b) rejection set forth above, specifically the rejection of claim 1 regarding the "(M x N) filter circuits" limitation, see below.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,002,435 issued to Yamamoto et al., hereinafter "Yamamoto".

Regarding **claim 1**, Yamamoto discloses a photodetector comprising:

(K.times.M.times.N) photodiodes PD.sub.k,m,n (K being an integer of no less than 2; k being integers of no less than 1 and no more than K; M being an integer of no less than 1; m being integers of no less than 1 and no more than M; N being an integer of no less than 2; and n being integers of no less than 1 and no more than N), each generating an electric charge by an amount corresponding to an intensity of light incident thereon *(refer to c. 13, ll. 51-60 and Figure 1, "100A", "120")*;

(M.times.N) integrating circuits, one of each being provided in correspondence to K photodiodes PD.sub.k,m,n (k=1 to K) among the (K.times.M.times.N) photodiodes PD.sub.k,m,n and each successively inputting and accumulating the electric charges generated at the K photodiodes PD.sub.k,m,n (k=1 to K) and outputting a voltage that is

in accordance with the amount of the accumulated electric charges *(refer to c. 14, ll. 14-19, c. 14, ll. 38-59, and Figure 1, "220")*; and

(M.times.N) filter circuits, one of each being provided in correspondence to each of the (M.times.N) integrating circuits and each reducing the thermal noise component contained in the voltage output from the corresponding integrating circuit and outputting the voltage alter reduction of the thermal noise component *(refer to c. 14, l. 60 - c. 15, l. 10 and Figure 1, "230")*.

Regarding **claim 4**, refer to the rejection of claim 1 and Yamoto further discloses that the (K.times.M.times.N) photodiodes PD.sub.k,m,n are arranged in M rows and (K.times.N) columns either two-dimensionally (when M=2) or one dimensionally (when M=1), with each photodiode PD.sub.k,m,n being positioned at the position of the m-th row and (n+(k-1)N)-th column *(refer to c. 18, ll. 31-65 and Figure 4)*.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-4 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of copending Application No. 10/539,067 (US Pub. No. 2006/0231748) in view of US Patent No. 6,002,435 issued Yamamoto et al, hereinafter "Yamamoto".

Regarding **claim 1 of the instant application**, claim 1 of Application No. 10/539,067 discloses all of the required limitations except for (M x N) filter circuits. As stated above, Yamamoto discloses the required limitations of claim 1 including (M.times.N) filter circuits, one of each being provided in correspondence to each of the (M.times.N) integrating circuits and each reducing the thermal noise component contained in the voltage output from the corresponding integrating circuit and outputting the voltage alter reduction of the thermal noise component *(filter could either be: (1) refer to c. 14, ll. 26-29, c. 15, ll. 11-26, and Figure 1, "230" which performs "impedance conversion" – examiner considers "impedance conversion" a filtering process; (2) alternatively refer to c. 14, ll. 29-31 and Figure 1, "250" which filters out the AC component, hence removing the noise associated w/ the DC component)*. Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to include a filter circuit as disclosed by Yamamoto in the photodetector disclosed by claim 1 of Application No. 10/539,067 in order to filter by either impedance conversion or filtering out an AC component.

Regarding **claim 2 of the instant application**, refer to claim 2 of Application No. 10/539,067.

Regarding **claim 3 of the instant application**, refer to claim 1 of Application No. 10/539,067.

Regarding **claim 4 of the instant application**, refer to claim 3 of Application No. 10/539,067.

This is a provisional obviousness-type double patenting rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following disclose the current state of the art in column or row readout of photodetectors:

Commonly assigned:

US Patent No. 6,956,607 issued to Mizuno et al.

US Patent No. 6,757,627 issued to Mizuno

US Patent No. 6,642,501 issued to Mizuno et al.

US Patent No. 6,075,564 issued to Mizuno

US Patent No. 6,606,123 issued to Mizuno

US Patent No. 6,700,110 issued to Mizuno et al.

US Patent No. 6,498,332 issued to Funakoshi

US Patent No. 5,731,578 issued to Mizuno

Not commonly assigned:

US Patent No. 6,031,570 issued to Yang et al.

US Patent No. 4,902,886 issued to Smisko

US Patent No. 7,440,017 issued to Endo et al.

US Patent No. 6,344,877 issued to Gowda et al.

US Patent No. 5,892,540 issued to Kozlowski et al.

US Patent No. 6,873,364 issued to Krymski

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD M. BEMBEN whose telephone number is (571)272-7634. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David L. Ometz/
Supervisory Patent Examiner, Art Unit 2622

RMB